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# Design an Implementation of 64-Bit Multiplier using Vedic Mathematics in Verilog

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**ABSTRACT:** Nowadays due to the growing demand for improving processor performance in handling the complex algorithms and multi functioning making the all-processor cores are going to integrate on single chip. Even though the burden on the processor is not reducing. In order to reduce this we should provide the coprocessor for supporting operations done by main processor, these coprocessors will perform numeric operation like addition, multiplication, DSP application, etc. The speed of the processor will depend on the speed of the coprocessors. Vedic mathematics is the ancient type of mathematics which are having unique technique of 16 formulas to find solution of various application in the fast way. The paper provides the details of a 64-bit vedic multiplier design based on Vedic Sutras like Urdhva Tiryakbhyam. The results show that the vedic sutras are applicable for multiplication operation. The arithmetic module implemented is most efficient in terms of delay reduction because of vedic sutras. Here we are designing an 64-bit vedic which was based on these maths using Verilog HDL and Synthesised in Xilinx ISE, found that it's having enhanced performance.

## I. INTRODUCTION

One of the arithmetic operations is multiplying one number by another. Operations like multiplication are mostly required functions, presently enforced in several DSPs for applications like convolution, FFTs, filters and ALU (Arithmetic Logic Unit) of Microprocessor. A recurrently preferred operation is multiplication, it's necessary to design multiplier with reduced delay and efficient power utilization. Arithmetic calculations are working for many operations considering from simple routine work such as counting or multiplying to advanced science and business calculations. Hence, there is requirement of a fast and effective arithmetic unit in computers. Array Multiplication takes less time when compared to the partial product parallel calculation method. The delay produced is the time required for the signals to pass through the gates of multiplication array. Booth multiplier uses massive booth arrays for multiplier designs and exponents calculations with prime speed that successively demands partial add and partial carry registers. Two n-bit operands multiplication employing a radix-4 booth recording multiplier factor wants around  $n\text{-bits}/(2k)$  clock cycles to get part of the final product, where k indicates the number of booth recorder adder stages. Urdhva Tiryakbhyam Sutra based "Verticalcrosswise Algorithm" can be used to design digital multiplier like the Array multiplier. The ancient formula(sutra) provides the way to find product of  $N \times N$ , of N bits each multiplicand by considering smaller parts of size  $(N/2 = n)$ , say.

## II. EXISTING SYSTEM

Vedic mathematics is part of four Vedas (books of wisdom). It is part of Sthapatya-Veda (book on civil engineering and architecture), which is an upa-veda (supplement) of Atharva Veda. It gives explanation of several mathematical terms including arithmetic, geometry (plane, co-ordinate), trigonometry, quadratic equations, factorization and even calculus. His Holiness Jagadguru Shankaracharya Bharati Krishna Teerthaji Maharaja (1884- 1960) comprised all this work together and gave its mathematical explanation while discussing it for various applications. Swamiji constructed 16 sutras (formulae) and 16 Upa sutras (sub formulae) after extensive research in Atharva Veda. Obviously these formulae are not to be found in present text of Atharva Veda because these formulae were constructed by Swamiji himself. Vedic mathematics is not only a mathematical wonder but also it is logical. That's why it has such a degree of eminence which cannot be disapproved. Due these phenomenal characteristics, Vedic maths has already crossed the boundaries of India and has become an interesting topic of research abroad. Vedic

maths deals with several basic as well as complex mathematical operations. Especially, methods of basic arithmetic are extremely simple and powerful.

1. (Anurupye) Shunyamanyat – If one is in ratio, the other is zero.
2. Chalana-Kalanabyham – Differences and Similarities.
3. Ekadhikina Purvena – By one more than the previous One.
4. Ekanyunena Purvena – By one less than the previous one.

These methods and ideas can be directly applied to trigonometry, plain and spherical geometry, conics, calculus (both differential and integral), and applied mathematics of various kinds. As mentioned earlier, all these Sutras were reconstructed from ancient Vedic texts early in the last century. Many Sub-sutras were also discovered at the same time, which are not discussed here. The beauty of Vedic mathematics lies in the fact that it reduces the otherwise cumbersome-looking calculations in conventional mathematics to a very simple one.

### III. PROPOSED SYSTEM

#### RTL Schematic Diagram Of Vedic Multiplier

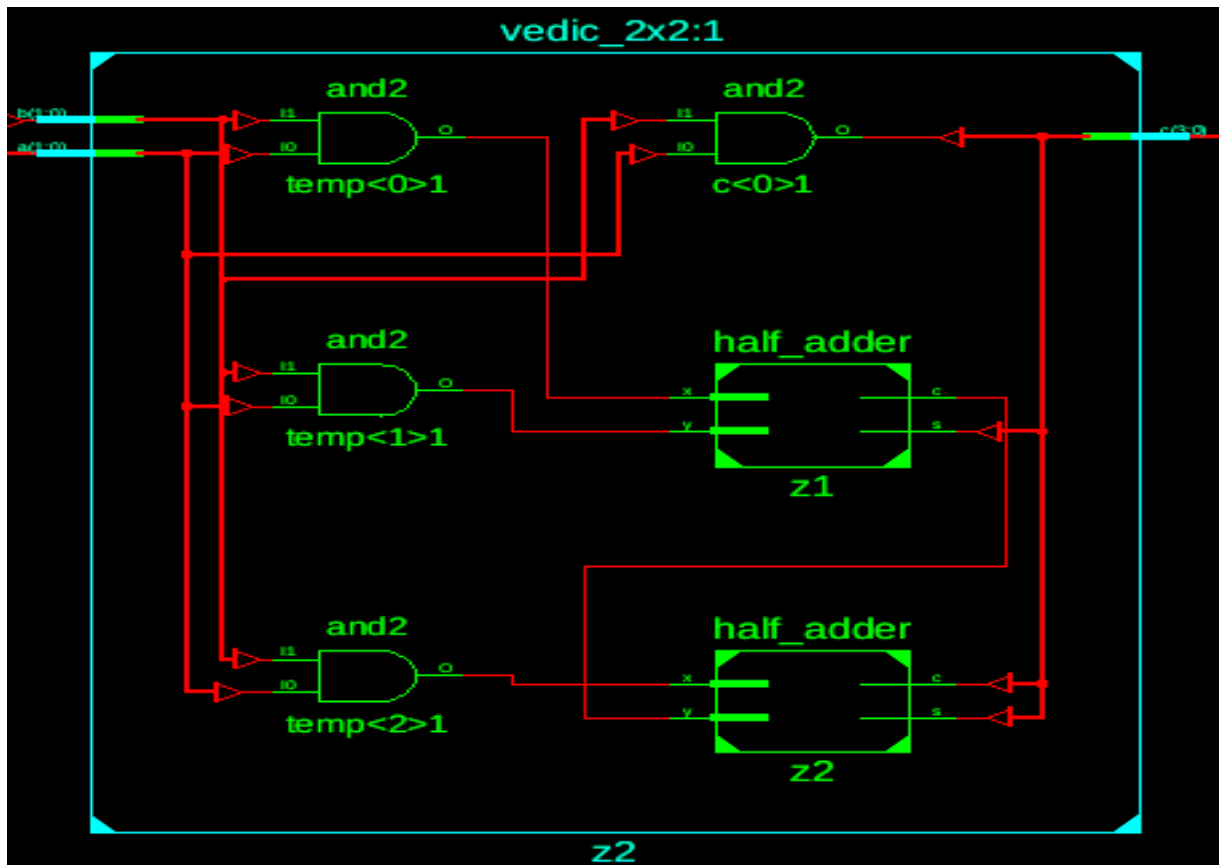


Fig: 3.1 RTL Internal diagram of Vedic 2x2 Multiplier.

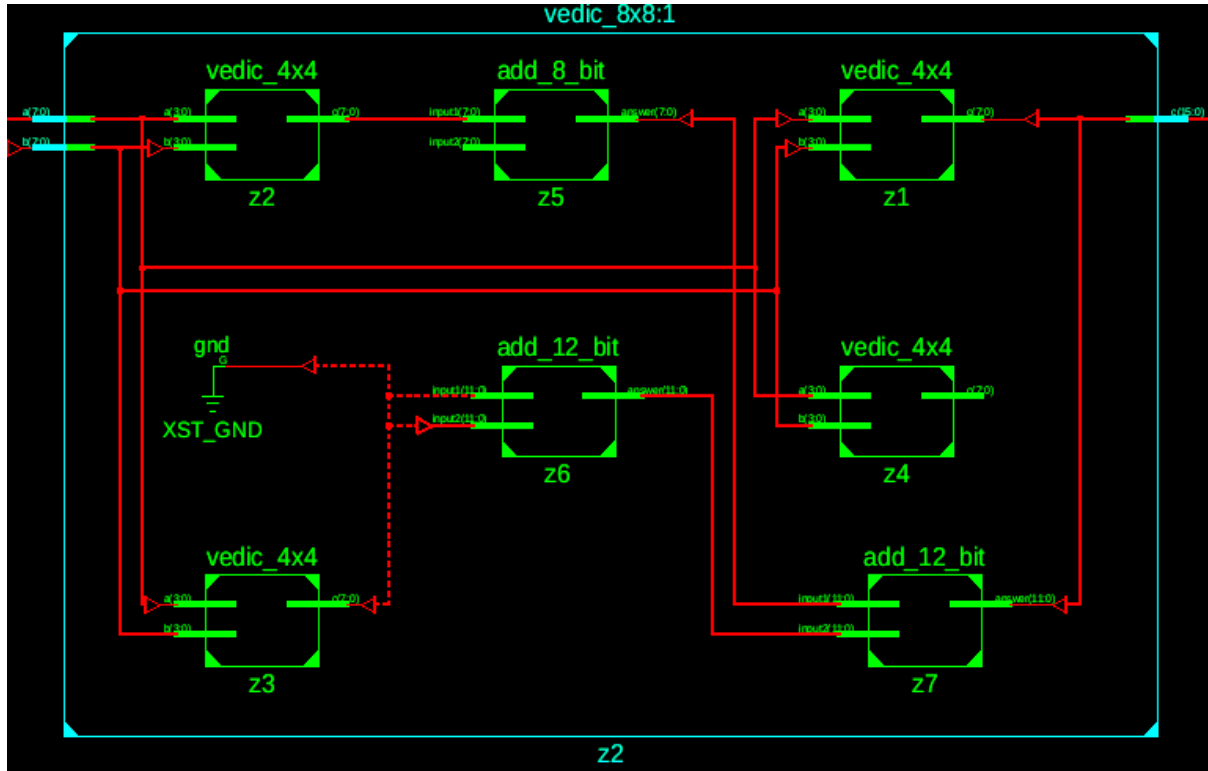


Fig : 3.2 RTL Internal diagram of Vedic 8x8 Multiplier.

#### IV. EXPERIMENTAL RESULT

The below figure-1, is the RTL Schematic diagram of 64x64 multiplier using Vedic Mathematics Here a, b are the inputs of the 64-bit multiplier and out is the output.

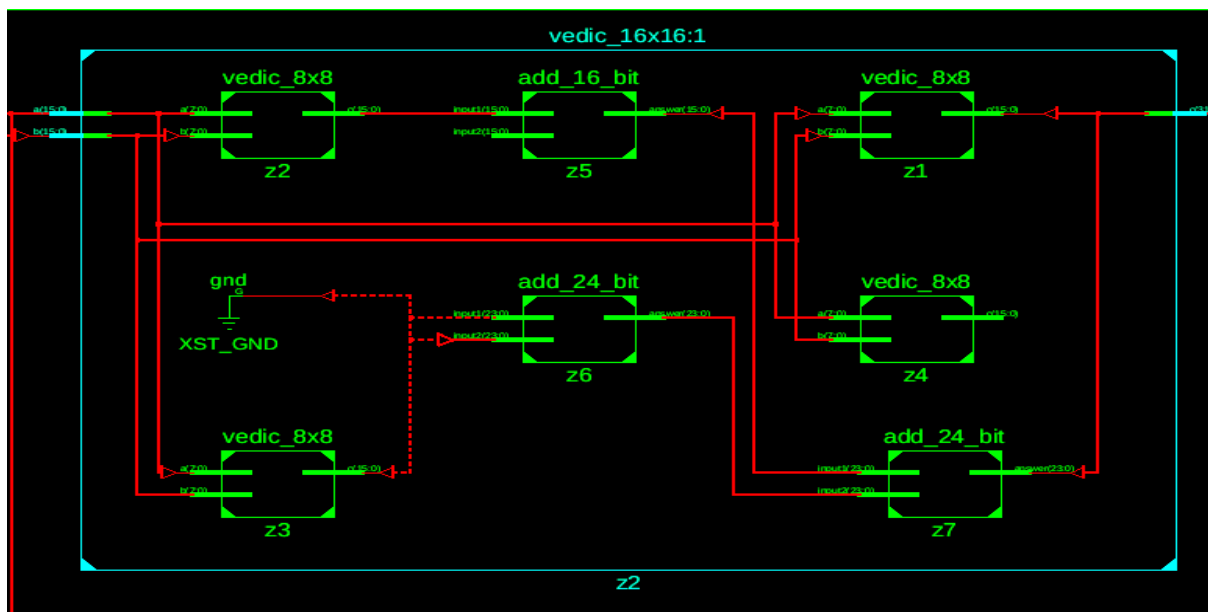


FIG: 4.1 RTL Internal diagram of Vedic 16x16 Multiplier.

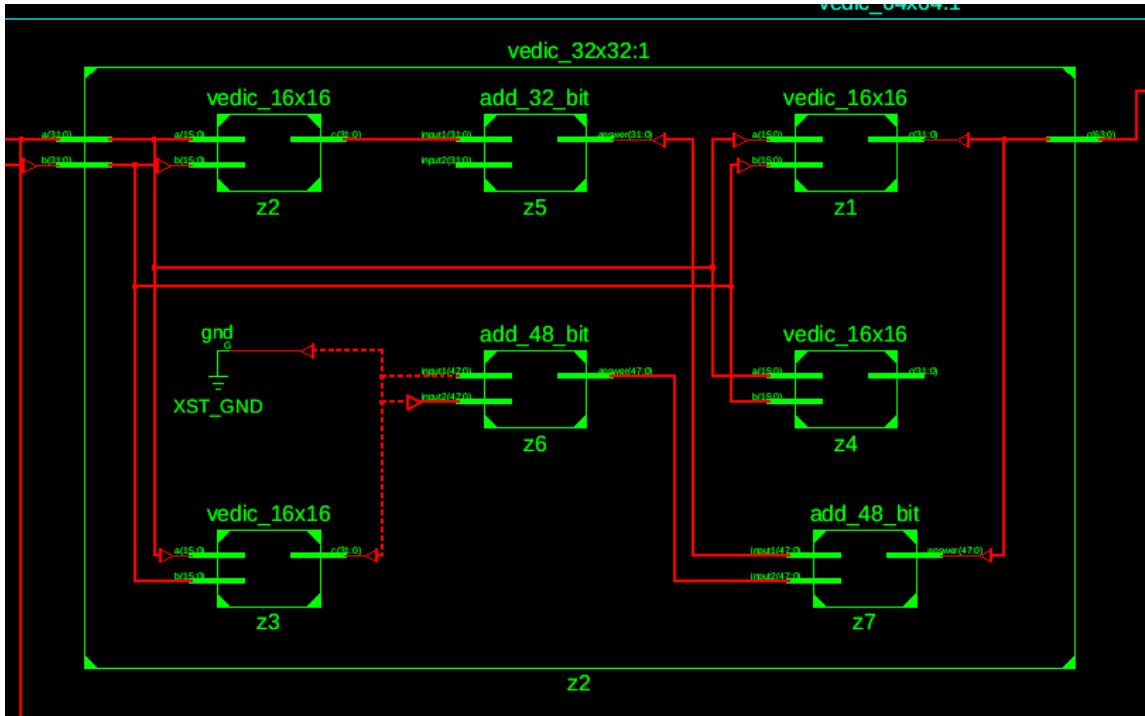


FIG: 4.2 RTL Internal diagram of Vedic 32x32 Multiplier.

SIMULATION RESULT OF VEDIC MULTIPLIER



FIG: 4.3 Simulation result of 64-Bit Vedic Multiplier

The above diagram-6, is the simulation result of final output here we have given input  $a=345$  and  $b=678$  then output  $out=233910$  this output is verified according to inputs in this way Vedic multiplier multiplies 64-bit numbers. The inputs we can give in the binary form also with selecting binary format then we have to select output as binary form. This result confirms the correct operation of the multiplier, as the product of 345 and 678 is indeed 233910. The correctness of this output validates the functionality of the Vedic multiplier in handling decimal inputs. More over, the Vedic multiplier supports both decimal and binary input formats. If the user prefers to work with binary values, they can choose the binary input format for both operands. In such cases, the output will also be generated in binary format, ensuring compatibility with digital systems and further simulation analysis. This simulation demonstrates the capability of the Vedic multiplier to perform accurate and efficient multiplication of 64-bit numbers using the Urdhva Tiryakbhyam (vertical and crosswise) method of Vedic mathematics, which is known for its high speed and optimized logic implementation in digital circuits. This implementation utilizes the **Urdhva Tiryakbhyam** Sutra (vertical and crosswise method) from ancient Vedic mathematics, which is particularly well-suited for high-speed arithmetic operations. The method decomposes the multiplication process into a series of parallel steps, allowing for faster computation compared to traditional shift-and-add algorithms. The architecture is inherently scalable, supports pipelining, and leads to an optimized logic footprint—making it ideal for applications in FPGA and ASIC designs where speed and area efficiency are critical. Overall, this simulation illustrates the efficiency, correctness, and flexibility of the Vedic multiplier in handling both small and large (up to 64-bit) data widths, while offering configurable input/output formats and enhanced performance for modern digital arithmetic applications.

## V. CONCLUSION

In this thesis, a 64-bit Vedic multiplier has been successfully implemented using the principles of Vedic Mathematics, specifically the Urdhva Tiryakbhyam Sutra. This ancient sutra, which translates to “Vertically and Crosswise,” forms the foundation of a highly efficient algorithm for multiplication. The approach is inherently parallel and scalable, making it particularly suitable for high-speed arithmetic operations in digital systems. The Urdhva Tiryakbhyam method simplifies the multiplication process by breaking it into smaller, more manageable operations that can be executed concurrently. As a result, the design exhibits reduced computational complexity and lower propagation delay when compared to conventional multiplication techniques such as Booth or array multipliers. This efficiency is especially critical in modern VLSI applications where speed and area are of utmost importance. Overall, this thesis demonstrates the effectiveness of integrating Vedic mathematical techniques in modern digital design. The Urdhva Tiryakbhyam Sutra proves to be a powerful tool for enhancing arithmetic operation performance, and its adoption can lead to more optimized, faster, and energy-efficient digital systems in real-time applications such as signal processing, cryptography, and embedded systems.

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